

Technical Note

Small-Block vs. Large-Block NAND Flash Devices

For detailed NAND Flash device information, see www.micron.com/products/nand/partlist.aspx.

Introduction

As NAND Flash densities increase, it has become necessary to organize the NAND Flash array more efficiently while simultaneously reducing cost. Increasing the block size of the NAND Flash array accomplishes both of these goals. Using fewer blocks increases READ, PROGRAM, and ERASE performance and reduces chip size by reducing peripheral circuits between blocks. Most newer NAND Flash designs use the large-block format.

A general rule for determining when NAND Flash devices transition from small-block to large-block organization is:

- Small-block devices \leq 1Gb density.
- Large-block devices \geq 1Gb density.

Array Organization

Small-block NAND Flash devices contain blocks made up of 32 pages, where each page contains 512 data bytes + 16 spare bytes. Large-block NAND Flash devices contain blocks made up of 64 pages, each page containing 2,048 data bytes + 64 spare bytes. For a 1Gb NAND Flash device, this translates to 8,192 blocks in the small-block organization and 1,024 blocks in the large-block organization.

These organizational differences are highlighted in Figures 1 and 2 on page 2 and in Table 1 on page 3.

Figure 1: 1Gb NAND Flash Small-Block Array Organization

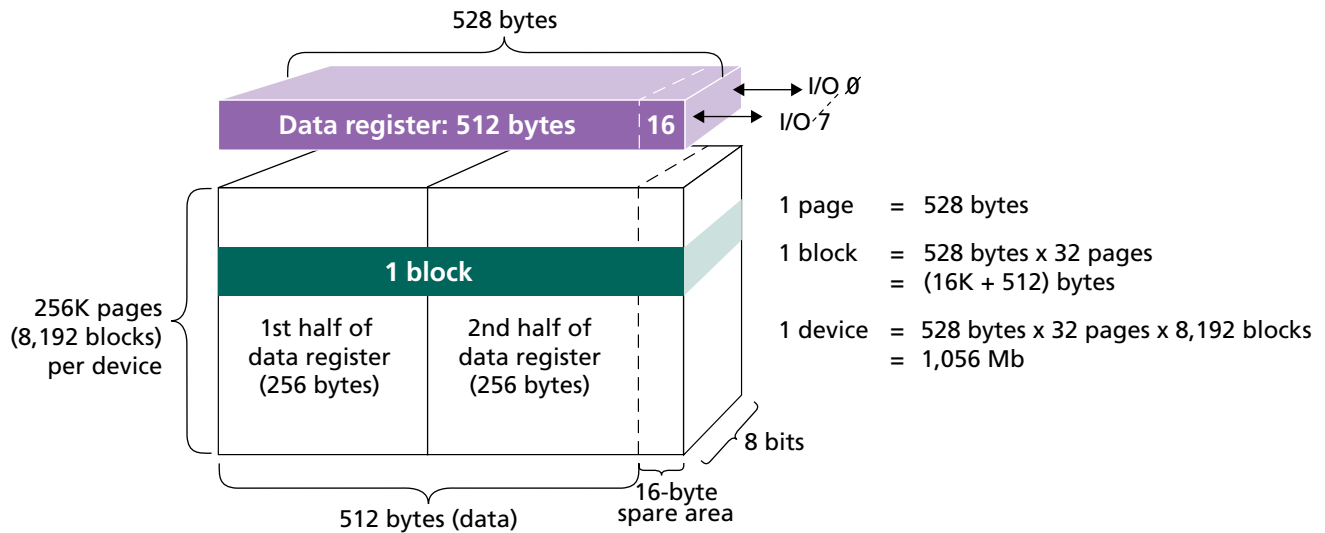


Figure 2: 1Gb NAND Flash Large-Block Array Organization

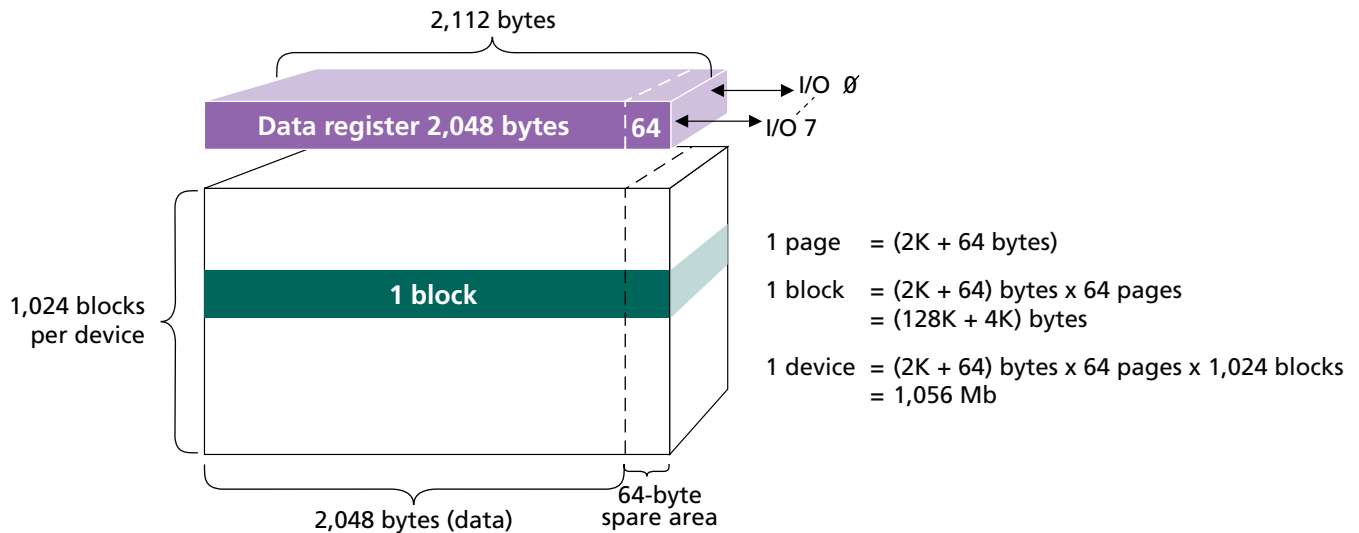


Table 1: Small-Block/Large-Block Comparison

Page #	Small Block	Large Block
0	512 bytes + 16 bytes	2,048 bytes + 64 bytes
1	512 bytes + 16 bytes	2,048 bytes + 64 bytes
2	512 bytes + 16 bytes	2,048 bytes + 64 bytes
...
30	512 bytes + 16 bytes	2,048 bytes + 64 bytes
31	512 bytes + 16 bytes	2,048 bytes + 64 bytes
32	N/A	2,048 bytes + 64 bytes
...
62	N/A	2,048 bytes + 64 bytes
63	N/A	2,048 bytes + 64 bytes
Total bytes	16,896	135,168

Address Cycles

NAND Flash devices have no dedicated address pins. Addresses are loaded via a shared I/O bus that is also used for loading commands and data. Small-block and large-block NAND Flash devices use 4 address cycles to load the entire address for a 1Gb device. However, as shown in Tables 2 and 3, the address cycles are used differently by small-block and large-block devices. The small-block devices use 1 column address cycle while the large-block devices require 2 column address cycles. Small-block devices require more row address cycles due to the increased number of blocks.

Large-block 2Gb devices use 5 address cycles.

Table 2: Small-Block NAND Flash Address Cycles

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	A7	A6	A5	A4	A3	A2	A1	A0
Second	A16	A15	A14	A13	A12	A11	A10	A9 ¹
Third	A24	A23	A22	A21	A20	A19	A18	A17
Fourth	LOW	LOW	LOW	LOW	LOW	LOW	A26	A25

Notes: 1. There is no A8 address bit in small-block devices.

Table 3: Large-Block NAND Flash Address Cycles

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA16

Commands

Some commands differ between small- and large-block NAND Flash devices. The system designer should be aware of these differences and implement accordingly. Table 4 shows the basic command set for small-block NAND Flash devices; Table 5 shows the basic command set for large-block devices.

Table 4: Small-Block NAND Flash Commands

Command	1st Cycle	2nd Cycle	3rd Cycle	Acceptable Command During Busy
READ 1	00h/01h	–	–	No
READ 2	50h	–	–	No
READ ID	90h	–	–	No
RESET	FFh	–	–	Yes
PAGE PROGRAM (actual)	80h	10h	–	No
PAGE PROGRAM (dummy)	80h	11h	–	No
COPY BACK PROGRAM (actual)	00h	8Ah	10h	No
COPY BACK PROGRAM (dummy)	03h	8Ah	11h	No
BLOCK ERASE	60h	D0h	–	No
MULTI-PLANE BLOCK ERASE	60h-60h	D0h	–	No
READ STATUS	70h	–	–	Yes
READ MULTI-PLANE STATUS	71h	–	–	Yes

Table 5: Large-Block NAND Flash Commands

Command	1st Cycle	2nd Cycle	Valid During Busy
PAGE READ	00h	30h	No
PAGE READ CACHE MODE START	31h	–	No
PAGE READ CACHE MODE START LAST	3Fh	–	No
READ for INTERNAL DATA MOVE	00h	35h	No
RANDOM DATA READ	05h	E0h	No
READ ID	90h	–	No
READ STATUS	70h	–	Yes
PROGRAM PAGE	80h	10h	No
PROGRAM PAGE CACHE MODE	80h	15h	No
PROGRAM for INTERNAL DATA MOVE	85h	10h	No
RANDOM DATA INPUT for PROGRAM	85h	–	No
BLOCK ERASE	60h	D0h	No
RESET	FFh	–	Yes

Operation Examples

General operation is similar in small-block and large-block NAND Flash devices. For example, when reading a page of data, both large- and small-block NAND Flash devices must first transfer a page of data from the NAND Flash array to the data register, as shown in Figure 3. The t_R parameter represents the time required to move the page of data from the NAND Flash array into the data register. When a page of data is being programmed in both large- and small-block NAND Flash devices, the data is clocked into the device serially and stored in the cache register until a PROGRAM CONFIRM command is issued; the NAND Flash array is then programmed with the data. The t_{PROG} parameter represents the time required to program the data from the data register to the NAND Flash array.

Figure 3: Small-Block/Large-Block PROGRAM and READ Operations

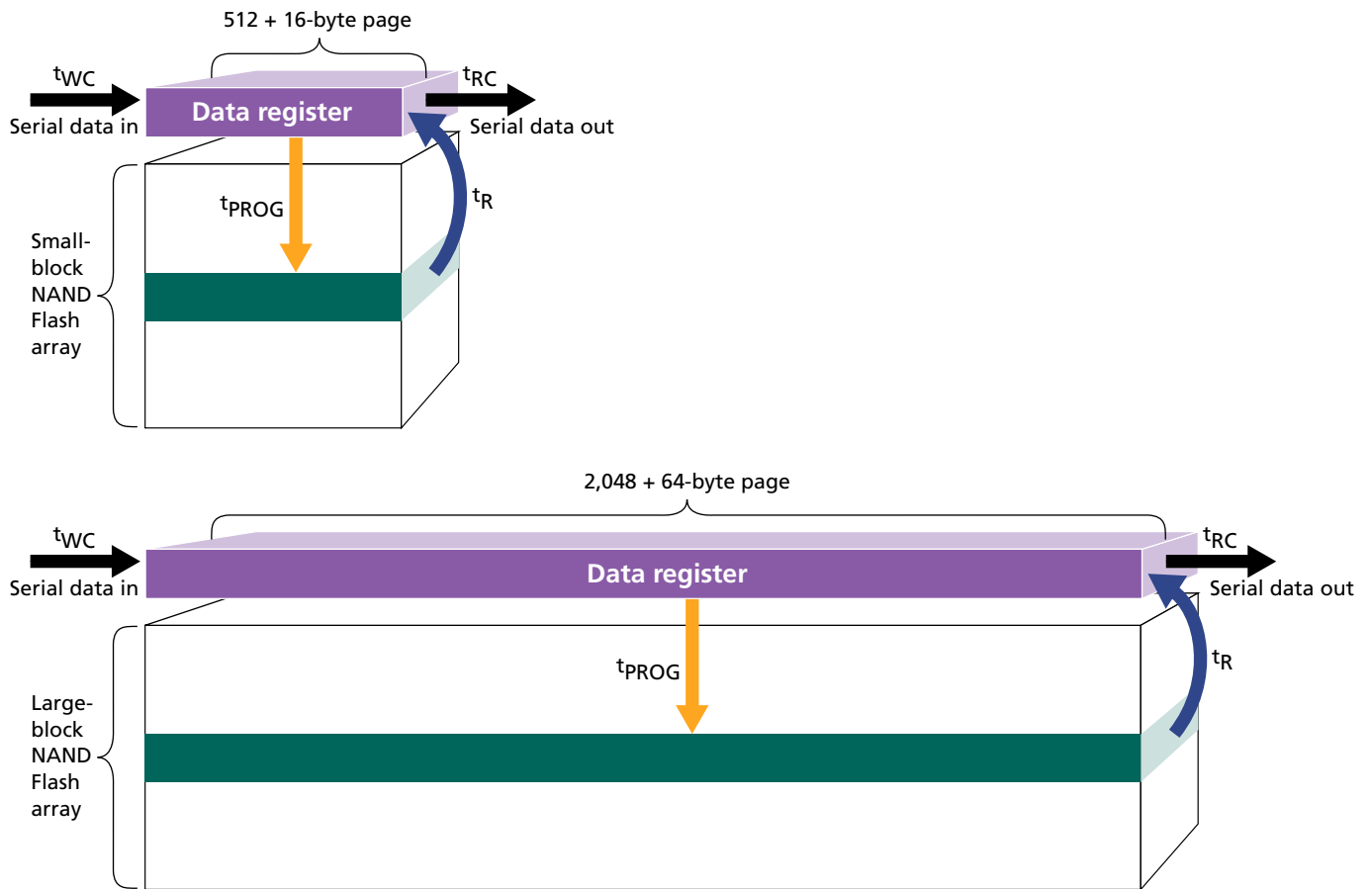


Table 6: PROGRAM and READ Operation Parameters

Symbol	Parameter Definition
t_{PROG}	Program time
t_R	Random access time
t_{RC}	Serial READ cycle time
t_{WC}	WRITE cycle time

READ Operations

Small-Block READ Operations

There are several important differences between small-block and large-block READ operations. Small-block NAND Flash devices use an 8-bit column address cycle that can access up to 256 unique bytes in a page. The page size is 512 bytes + 16 spare bytes, so the small-block device must use three address pointer commands to access all the bytes in the page. This leads to a more complicated method for accessing the NAND Flash array. As shown in Figures 4 and 5, and in Figure 6 on page 7, the address pointer is set by the command used to read the NAND Flash array:

- The 00h command sets the pointer to the A area, consisting of bytes 0–255.
- The 01h command sets the pointer to the B area, consisting of bytes 256–511.
- The 50h command sets the pointer to the spare C area, consisting of bytes 512–527.

Figure 4: Small-Block READ 1 Operation, Command 00h

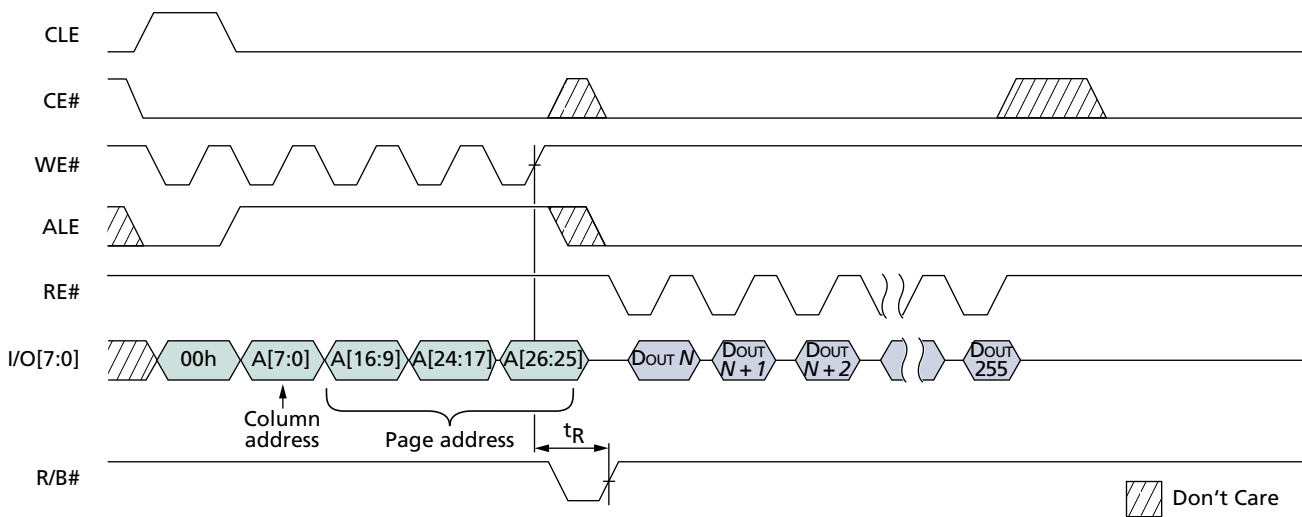


Figure 5: Small-Block READ 1 Operation, Command 01h

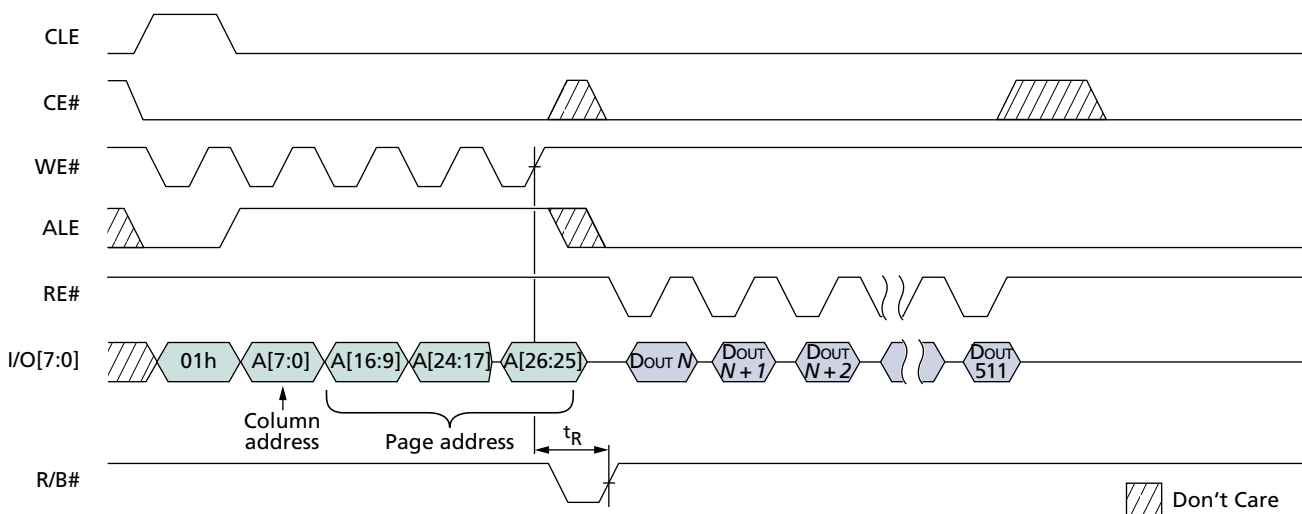
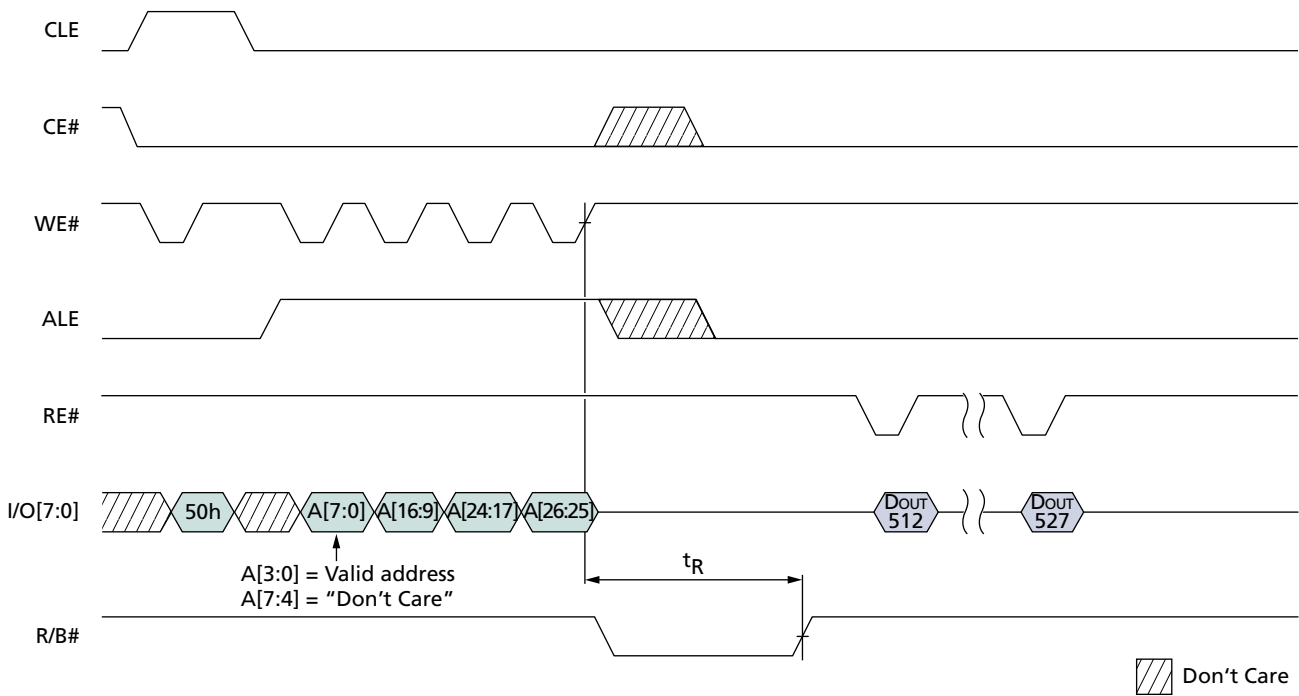


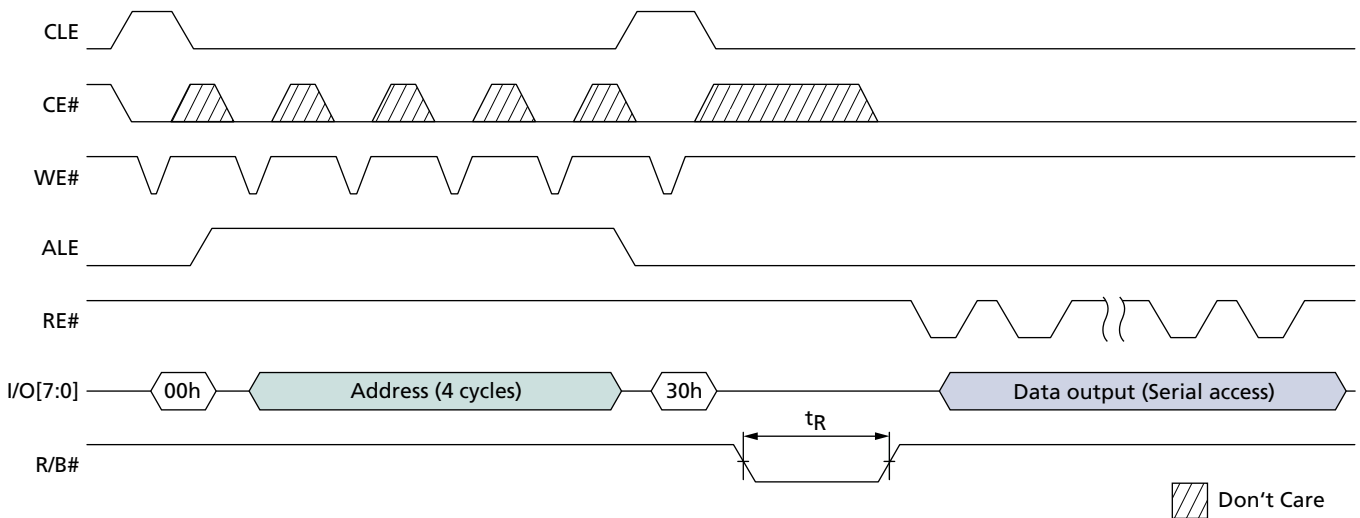
Figure 6: Small-Block READ 2 Operation



Large-Block READ Operations

Large-block NAND Flash devices offer a simplified approach to accessing the NAND Flash array for READ operations. A PAGE READ command consists of a single command, 00h, followed by 4 address cycles for a 1Gb device, and a READ CONFIRM command, 30h, regardless of the area accessed in the NAND Flash array (see Figure 7).

Figure 7: Large-Block PAGE READ Operation



PROGRAM Operations

Small-Block NAND Flash PROGRAM Operations

Small-block NAND Flash devices also use an address pointer for programming operations. Implementing the address pointer for PROGRAM operations is similar to implementing the address pointer for READ operations:

- The 00h command sets the pointer to the A area, consisting of bytes 0–255.
- The 01h command sets the pointer to the B area, consisting of bytes 256–511.
- The 50h command sets the pointer to the spare C area, consisting of bytes 512–527.

Figure 8: Area A PROGRAM Command Input Sequence

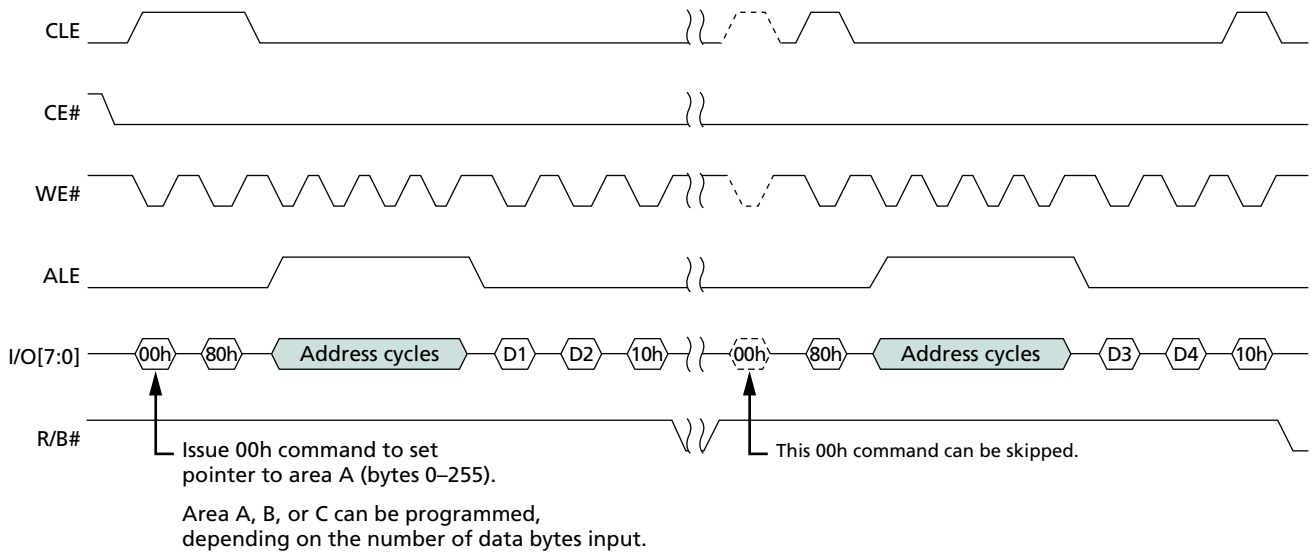


Figure 9: Area B PROGRAM Command Input Sequence

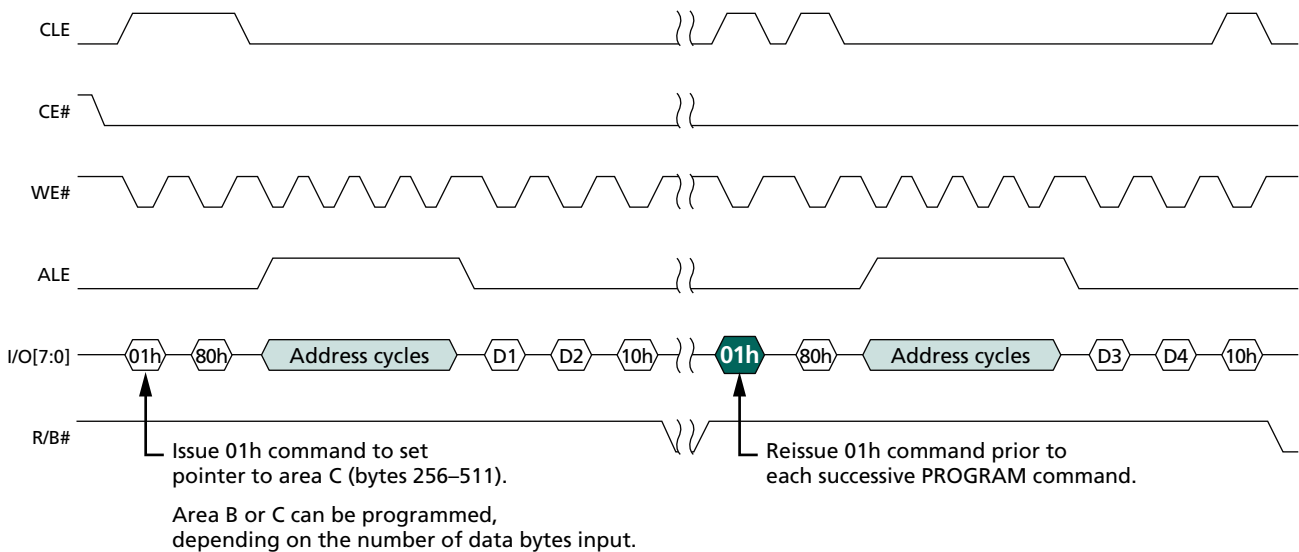
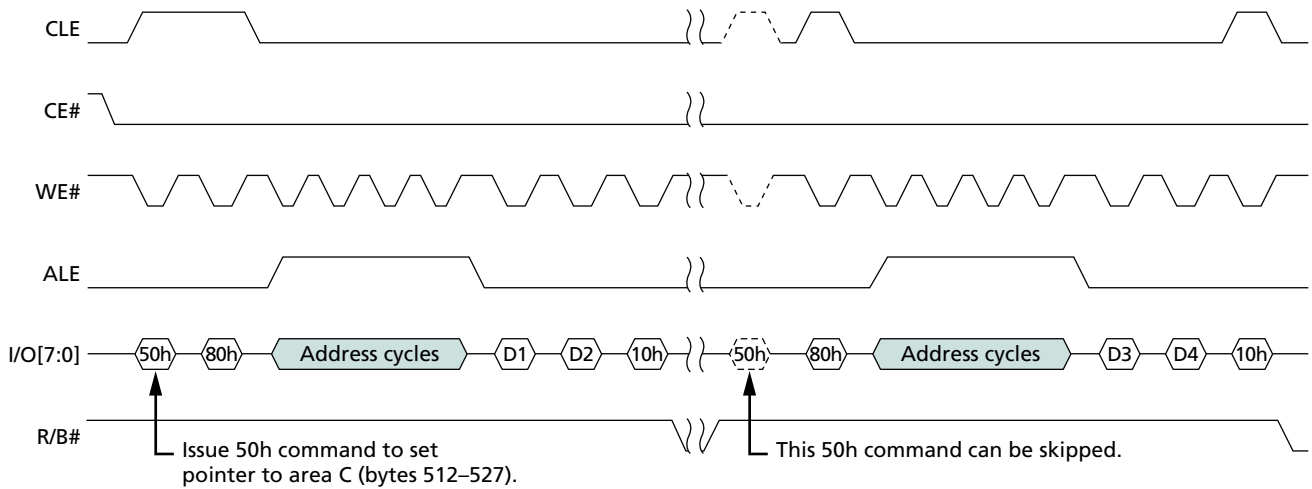


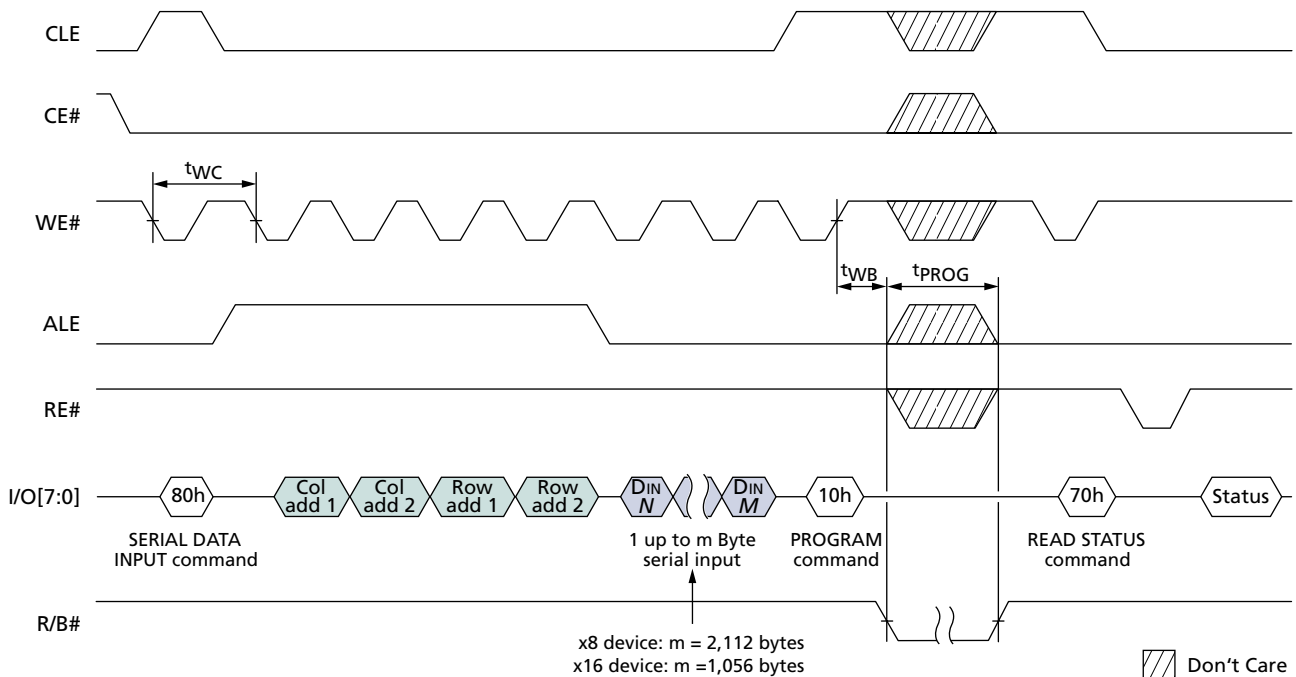
Figure 10: Area C PROGRAM Command Input Sequence



Large-Block NAND Flash PROGRAM Operations

Large-block NAND Flash devices offer a simplified approach to programming the NAND Flash array. A PROGRAM PAGE command consists of an 80h command followed by 4 address cycles (for a 1Gb device), and a PROGRAM CONFIRM command, 10h, regardless of the area accessed in the NAND Flash array; no special address pointers are required. This simplifies the software interface for the NAND Flash device (see Figure 11).

Figure 11: Large-Block PROGRAM Operations



ERASE Operations

NAND Flash ERASE Operations

ERASE operations are similar for small-block and large-block NAND Flash devices. ERASE commands operate on one block at a time, so only row address cycles are required. In the case of a 1Gb device, the small-block NAND Flash device requires 3 address cycles; the large-block NAND Flash device requires only 2 address cycles (see Figures 12 and 13).

Figure 12: Small-Block ERASE Operation

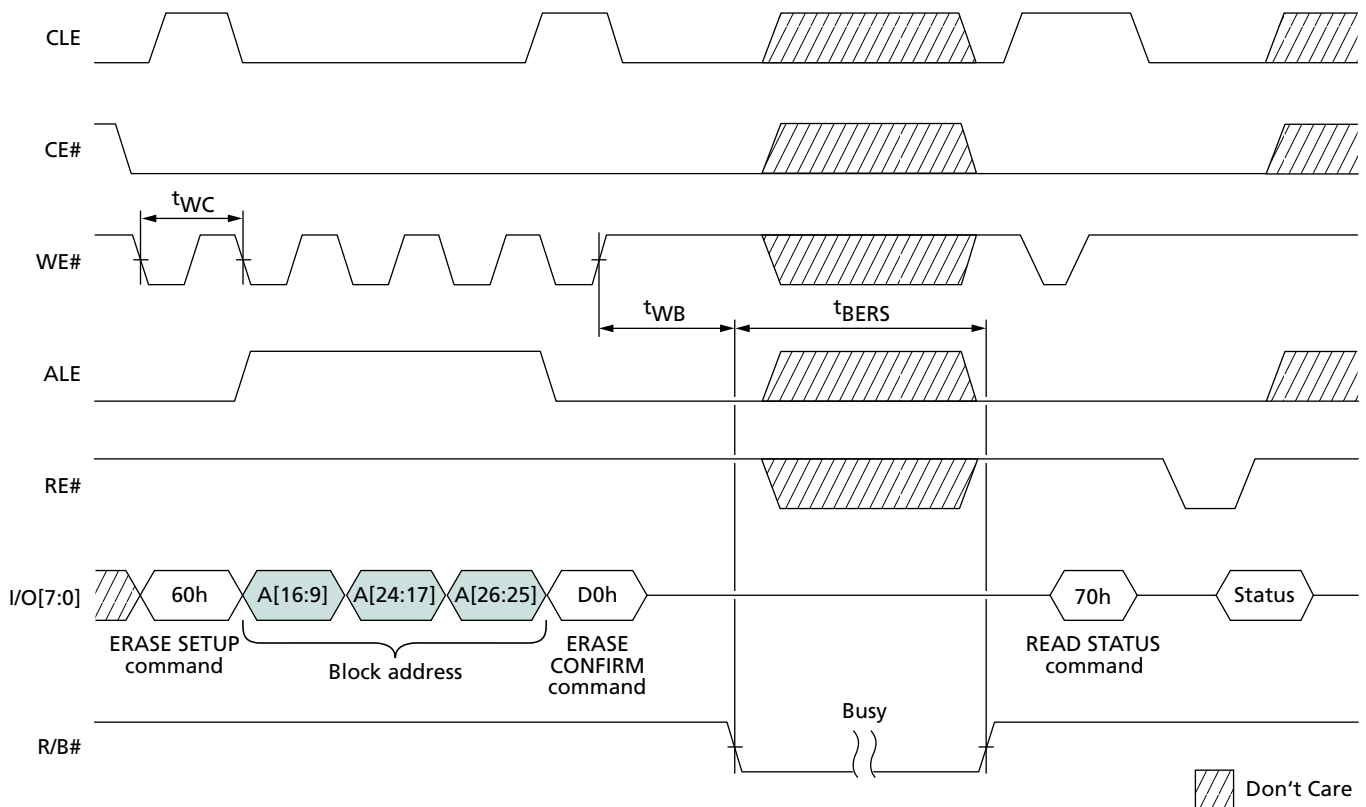
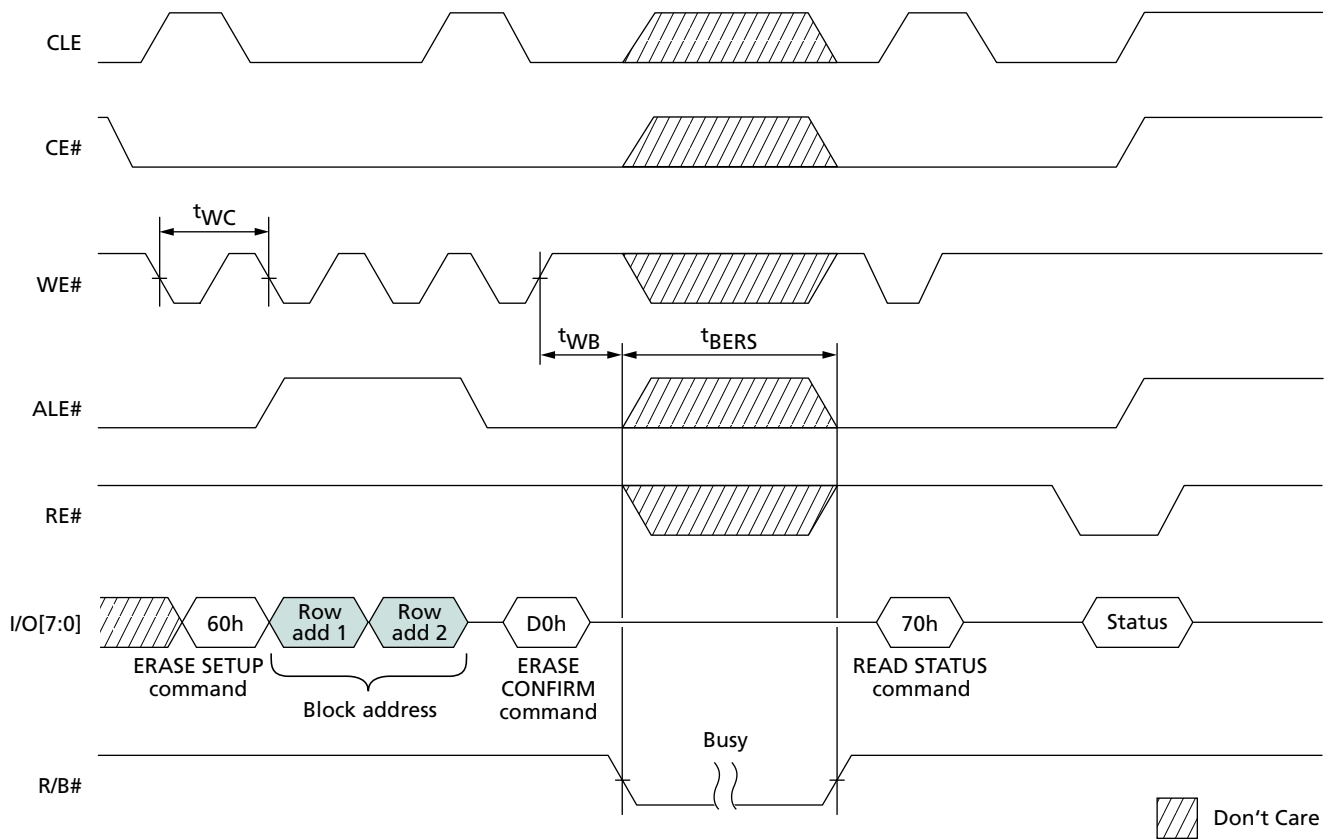


Figure 13: Large-Block ERASE Operation



Performance Comparison

Large-block NAND Flash devices offer increased READ, PROGRAM, and ERASE performance compared to their small-block counterparts. Tables 7, 8, and 9 provide comparisons for each operation.

Table 7: READ Performance: Small Block vs. Large Block

Process	Small Block			Large Block			Unit
	Repetitions	Cycle Time	Total Time	Repetitions	Cycle Time	Total Time	
Command latch (00h and/or 01)	2	50	100	1	50	50	ns
Address latch	4	50	200	4	50	200	ns
Command latch (30h or 50h)	1	50	50	1	50	50	ns
R/B# LOW (^t R)	1	15	15	1	25	25	μs
Data output cycles	528	50		2,112	50		ns
Data output cycles total time			26.4			105.6	μs
Total time to read a page			41.75			130.9	μs
Data rate			12.65			16.13	MB/s

Table 8: PROGRAM Performance: Small Block vs. Large Block

Process	Small Block			Large Block			Unit
	Repetitions	Cycle Time	Total Time	Repetitions	Cycle Time	Total Time	
Command latch (80h)	2	50	100	1	50	50	ns
Address latch	4	50	200	4	50	200	ns
Command latch (10h)	1	50	50	1	50	50	ns
R/B# LOW (^t PROG)	1	200	200	1	300	300	μs
Data input cycles	528	50		2,112	50		ns
Data input cycles total time			26.4			105.6	μs
Total time to program a page			226.75			405.9	μs
Data rate			2.33			5.20	MB/s

Table 9: ERASE Performance: Small Block vs. Large Block

Block	Block Size	ERASE Time per Block	Unit
Small	16K	2	ms
Large	128K	2	ms

Summary

Large-block NAND Flash devices offer significant performance increases over their small-block NAND Flash counterparts for READ, PROGRAM, and ERASE operations. In addition, large-block NAND Flash devices can access various parts of the NAND Flash array without address pointers. This provides greater flexibility for system designers, simplifies the software interface for the NAND Flash device, and decreases overhead for command and address operations. Most newer NAND Flash designs utilize large-block format.



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Revision History

Rev. C **5/07**

- “Introduction” on page 1: Revised description.
- Table 3 on page 3: Changed cycle 3 and 4 values.
- “Operation Examples” on page 5: Changed “cache register” to “data register” in the second, third, and last sentences.

Rev. B **2/06**

- Table 7 on page 12: Changed “Read data cycles” and “Read data cycles total time” to “Data output cycles” and “Data output cycles total time.” Changed “Total time to program a page” to “Total time to read a page.”

Rev. A **3/05**

- Initial release.